# A high supply voltage bandgap reference circuit using drain-extended MOS devices

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**Abstract:** A bandgap reference circuit that uses high-voltage drain-extended MOS (DeMOS) devices is presented for high supply voltage application without using a voltage regulator for the bandgap core circuit. The bandgap reference circuit was fabricated using commercially available $0.18\,\mu$m high-voltage DeMOS technology. Measurement result of the chip shows that the reference voltage change rate for VDD variation from 5 V to 30 V and for the temperature variation from $-40°$C to $+140°$C were $1.16\,$mV/V and $0.84\,$mV/°C, respectively. The measured reference voltage with the supply voltage of 15 V at room temperature was $2.487\,$V. The current consumption and the active area were $3.2\,\mu$A and $320 \times 345\,\mu$m$^2$, respectively.

**Keywords:** bandgap reference, high-voltage, drain extended CMOS, DEMOS, BGR

**Classification:** Integrated circuits

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## 1  Introduction

Bandgap reference circuits, after the work reported in [1], are used almost of all the analog and analog-mixed signal ICs in order to provide reference voltage(s) for the internal circuits of the ICs where reference voltages are required. The realization of a bandgap reference circuits is usually done with supply voltage less than 5 volts [1, 2, 3]. For some applications, the supply voltage to the core circuit of the reference generator was regulated in order to improve PSRR and/or meet the maximum voltage requirement for the given process [4, 5]. Introducing a regulator increases power consumption as well as the complexity of the circuit. In applications requiring small-size and low-power, therefore, a bandgap reference circuit without using voltage regulator for bandgap core circuit requires, while maintaining good robustness against power-supply noise and wide supply voltage range.

In [6], a bandgap reference circuit that uses a high-voltage SOI MOS transistors was proposed. The circuit structure was implemented efficiently for wide power-supply voltage ranges without applying a regulator for the bandgap core circuit by using high-voltage SOI nMOS in one of the branch out of four branches. But, it adopted asymmetrical biasing scheme due to difficulties of achieving high-voltage p-channel transistors. The circuit have a large stack of p-channel transistors for reference current generation, which limits the minimum supply voltage value. A circuit structure similar to this work was reported in [7] for high-voltage applications, but the standard CMOS transistors were assumed to implement the reference circuit. When the circuit structure in [7] is simulated with high supply-voltage DeMOS transistors only, the reference voltage variation at high temperature is significant as shown in Figure 2 (a). The leakage impact of DeMOS device on the reference voltage at high temperature is also reported in [8] due to large junction area and intrinsic carrier density.

This paper presents the result of fabrication of a bandgap voltage reference circuit using both high-voltage DeMOS devices and low-voltage MOS devices.

## 2  Proposed bandgap reference circuit

A bandgap reference voltage ($V_{BG}$) can be formed by a linear combination of base-emitter voltage of bipolar transistor ($V_{BE}$) and the voltage difference of two different bipolar transistors ($\Delta V_{BE}$), i.e., $V_{REF} = \alpha_1 V_{BE} + \alpha_2 \Delta V_{BE}$ [9].
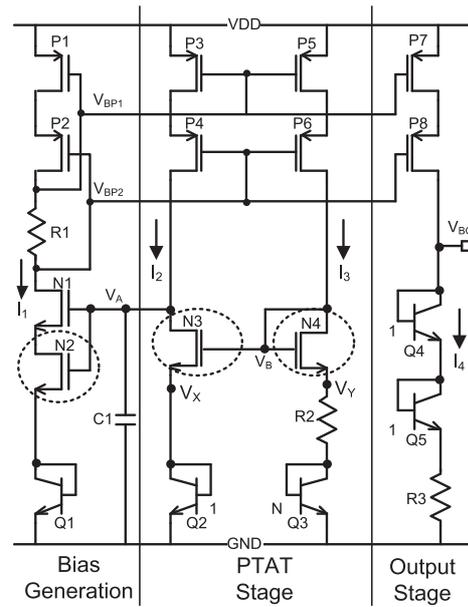
**Fig. 1.** The proposed bandgap reference circuit. The nMOS devices inside circles are low-voltage devices, and all other devices are DeMOS transistors.

Since $V_{BE}$ and $\Delta V_{BE}$ have negative (CTAT) and positive (PTAT) temperature coefficient, respectively, temperature dependence of the voltage can be minimized by choosing proper value of $\alpha_1$ and $\alpha_2$.

Figure 1 shows the bandgap reference circuit used in this work. The reference voltage target of this work was 2.48 V, and it is generally difficult to get this voltage using only one diode connected bipolar transistor. One way to resolve this issue is to stack two bipolar transistors, but stacking is not possible when there are any shared terminals between two transistors. Since the bipolar transistors can be isolated in the technology used here, we used a stack of two diode connected bipolar transistors, $Q_4$ and $Q_5$ as shown in Figure 1.

When the circuit is in a stable operating condition, $I_1 = I_3 = I_2$ and $V_X$ is the same as $V_Y$, the voltage across the $R_2$ is the same as $\Delta V_{BE}$, and the PTAT current $I_3$ equals to $V_T \ln(N)/R_2$. Therefore, $V_{BG}$ is expressed as in equation (1),

$$V_{BG} = 2V_{BE} + \frac{kT}{q}\ln(N)\left(\frac{R_3}{R_2}\right) \tag{1}$$

where $T$ is absolute temperature, $q$ is the charge of an electron, $k$ is Boltzmann's constant, $N$ is the emitter area ratio of $Q_3$ to $Q_2$, and $kT/q$ ($= V_T$) is thermal voltage which is about 26 mV at room temperature.

Assuming that $V_{BE}$ of both bipolar transistors $Q_4$ and $Q_5$ are equal, taking the partial derivative of equation (1) with respect to the temperature, we get

$$\frac{\partial V_{BG}}{\partial T} = 2\frac{\partial V_{BE}}{\partial T} + \frac{\partial V_T}{\partial T}\ln(N)\frac{R_3}{R_2} \tag{2}$$

To generate desired bandgap reference voltage that has less impact on tem-

perature, the relationship between $N$, $R_2$, and $R_3$ can be chosen after letting $\partial V_{BG}/\partial T = 0$ in the equation (2).

In the circuit, the nMOS transistors in the circle are low-voltage MOS transistors, and the rest of the MOS transistors are high-voltage DeMOS transistors. The maximum operating voltage for nMOS and DeMOS are 5 and 40 volts, respectively, while the maximum gate-source voltage for all MOS transistors and operating voltage of the bipolar transistors are 5 V. The role of the leftmost branch is to generate reference current and bias voltage for the cascode current mirror composed by pDeMOS P3, P4, P5, and P6. To make sure all the MOS transistors in the circuit operate in saturation region, the resistance $R_1$ in the bias generation branch is chosen to meet the relationship in equation (3).

$$|V_{GSP1}| - |V_{THP1}| \leq \frac{kT}{q}\ln(N)\frac{R_1}{R_2} \leq |V_{THP2}| \qquad (3)$$

where $V_{THP1,2}$ are the threshold voltages of pDeMOS P1 and P2, respectively.

The current determined by the leftmost branch is copied to the rest of the branches that results in all the branch currents are to be equal. Since the gain of voltage-current feedback loop composed by $V_A$, $I_1$, $V_{BP1,2}$, and $I_3$ is negative, a stable reference voltage generation can be achieved over the wide power-supply range. Based on the simulation result shown in Figure 2, the low-voltage nMOS transistors, $N_2$, $N_3$, and $N_4$, are used to alleviate the impact of nDeMOS leakage current impact at high temperature on the branch currents marked by $I_1$, $I_2$, and $I_3$, respectively. The nDeMOS $N_1$ is used to prevent the drain-source voltage of $N_2$, $V_{DS2}$, from exceeding its normal operating voltage. The purpose of capacitance $C1$ is to ensure that the feedback loop is stable, and it is implemented with low-voltage nMOS capacitance.

## 3   Experimental results

The bandgap reference circuit described in Section 2 was implemented with a combination of high-voltage DeMOS devices and low-voltage nMOS devices using a commercial $0.18\,\mu$m DeMOS process. The value of $R_1$ has chosen to be $120\,\text{K}\Omega$ for ensuring the devices in the circuit operate in saturation region. The values of $N$ and $R_2$ were chosen to be 8 and $65\,\text{K}\Omega$, respectively. To generate $2.48\,\text{V}$ reference voltage the ratio of $R_3/R_2$ was chosen according to the equation (2). The current of each branch was designed to be $0.8\,\mu$A, resulting in the total bandgap core current of $3.2\,\mu$A for the typical process parameter at VDD of 15 V. The capacitance $C_1$ used in this work was $2\,\text{pF}$.

Figure 2 shows the HSPICE simulation result of the temperature behavior of the reference voltage for the typical process corner. In Figure 2, the curves marked by solid square and circle are the simulation result of the circuits described in Section 2 and reported in [7], respectively. The reference voltage deviation at high-temperature using DeMOS devices for all the MOS devices in the circuit is observed with the circuit reported in [7] due to the large
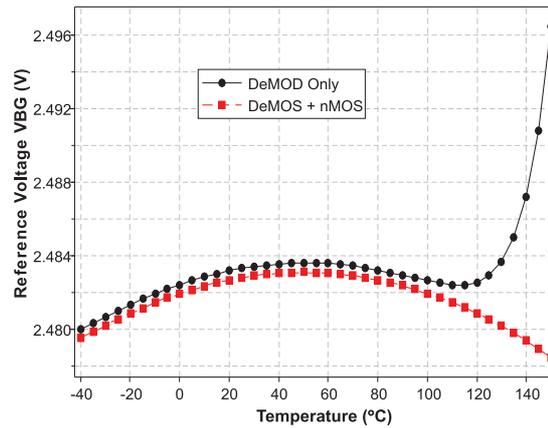
**Fig. 2.** Simulation result of the reference voltage variation over temperature. (a) The circuit using DeMOS only. (b) The circuit proposed in this work.
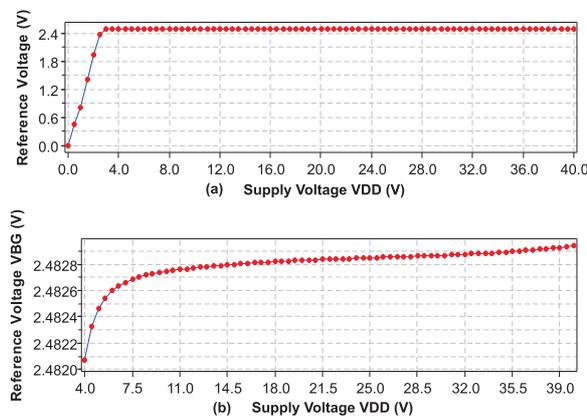


**Fig. 3.** Simulation result of the reference voltage variation over power-supply voltage at room temperature.

leakage current of nDeMOS devices at high-temperature impacting on the output branch.

Figure 3 shows the simulation result of the bandgap reference voltage variation over power-supply voltage for the typical process corner. Figure 3 (b) is the magnified version of 3 (a) in the power-supply range from 4 V to 40 V. As shown in the figure, the reference voltage behaviors well for wide range of power-supply voltage. The microphotograph of the fabricated bandgap reference circuit is shown in Figure 4, and the active area was $320 \times 345\,\mu m^2$.

The measurement result of $V_{BG}$ over power supply range from 5 V to 30 V is shown in Figure 5. The line marked by square represents the average value of $V_{BG}$ with twenty package samples, and lines marked by triangle and diamond represent the maximum and minimum values for all measured reference voltages, respectively. As shown in the Figure 5, the average $V_{BG}$ at 15 V was 2.487 V, and the $V_{BG}$ change over the supply range of 5 V~30 V was 1.16 mV/V.

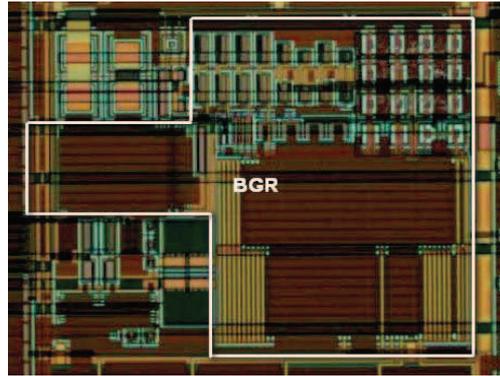Figure 6 shows the reference voltage deviation over the temperature range

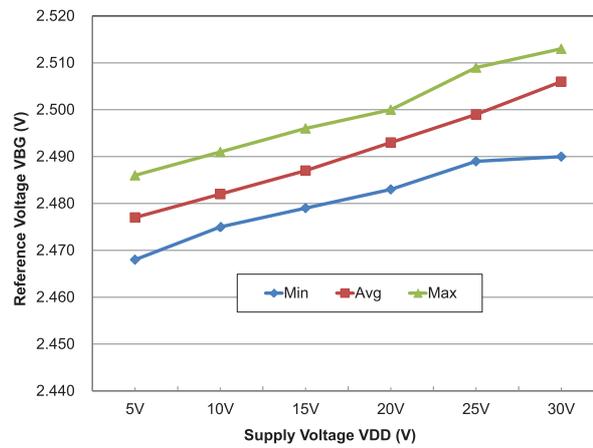**Fig. 4.** Microphotograph of the bandgap reference circuit.
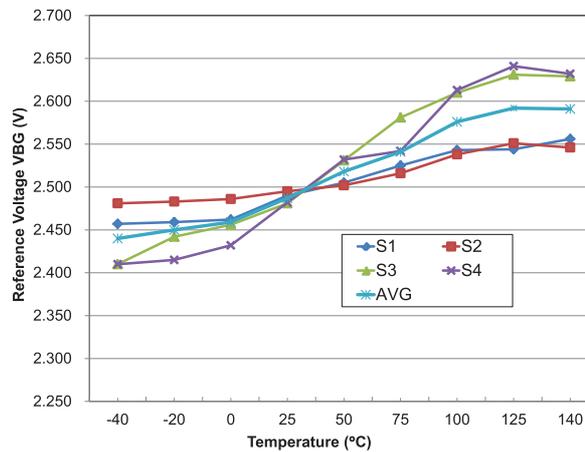


**Fig. 5.** Measured result of $V_{BG}$ with respect to VDD.



**Fig. 6.** Measured result of $V_{BG}$ with respect to temperature.

of $-40°$C$\sim$$140°$C. To measure the temperature dependency, we randomly selected four samples from the samples used for the VDD dependency measurement. The average change rate of $V_{BG}$ for the temperature was $0.84$ mV/$°$C.

## 4   Conclusions

We presented a bandgap reference circuit using a combination of high-voltage DeMOS and low-voltage MOS devices, and it was fabricated in a commercially available $0.18\,\mu$m high-voltage DeMOS process. The measured result shows that the average reference voltage of the fabricated circuit was 2.487 V with VDD of 15 V at room temperature. The reference voltage deviation for the supply variation from 5 V to 30 V was 1.16 mV/V, and for the temperature variation from $-40°$C to $+140°$C was 0.84 mV/°C. The proposed bandgap reference circuit was used in an IC with VDD of 15 V for controlling AC/DC adaptor system that requires low-power consumption.

## Acknowledgements